All-Graphene Three-Terminal-Junction Field-Effect Devices as Rectifiers and Inverters

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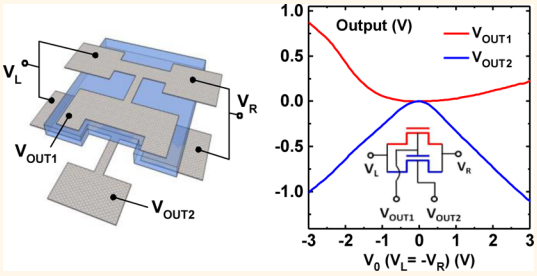
ABSTRACT We present prominent tunable and switchable room-temperature rectification performed at 100 kHz ac input utilizing micrometer-scale three-terminal junction field-effect devices. Monolayer CVD graphene is used as both a channel and a gate electrode to achieve all-graphene thin-film structure. Instead of ballistic theory, we explain the rectification characteristics through an electric-field capacitive model based on self-gating in the high source−drain bias regime. Previously, nanoscale graphene three-terminal junctions with the ballistic (or quasi-ballistic) operation have shown rectifications with relatively low efficiency. Compared to strict nanoscale requirements of ballistic devices, diffusive operation gives more freedom in design and fabrication, which we have exploited in the cascading device architecture. This is a significant step for all-graphene thin-film devices for integrated monolithic graphene circuits.



KEYWORDS: graphene · rectifier · inverter · transparent · CVD

Charge carrier transport in a two-dimensional electron gas (2-DEG) has been widely studied for the past decades to exploit its nonlinear properties arising in the ballistic regime.[1−14] Owing to the entirely two-dimensional lattice and exceptional electronic properties, graphene has recently attracted attention as a 2-DEG material. Recent developments on chemical vapor deposition (CVD) of continuous monolayer graphene enable cost-effective synthesis, and this has resulted in increased interest also in the industry.[15−18] Graphene field-effect transistors (GFETs) are among the most studied device structures for future electronic applications due to transparency, flexibility, and high carrier mobility.[19−21] Recently, state-of-the-art GFET structures have surpassed the gigahertz limit not only on a conventional rigid substrate such as Si but even on flexible substrates.[20,22−24] However, the transistor performance as a switch or rectifier is limited due to the zero band gap in graphene.

Exploiting nonlinear behaviors arising in the two-dimensional transport regime, electrical rectification on three-terminal junctions (TTJs) has also been demonstrated using exfoliated and silicon carbide graphene.[25−29] Nanoscale TTJs of conventional 2-DEG materials (*i.e.*, heterojunction of III−V semiconductors) are typically fabricated utilizing T-branch structures as the center branch, and structural symmetry is conveniently achieved in the device fabrication.[7−10] Rectification arises at the center of the channel due to the conductance difference between the left and right channels when two terminals are antisymmetrically biased (the so-called push−pull application). This is a result of the change of chemical potentials at the contacts by the bias voltage, which results in a shift of the potential symmetry point in the channel.[25] The nonlinear ballistic behavior can be explained by the Landauer−Büttiker formalism and is known to be a key mechanism for rectification on the nanoscale within a low push−pull voltage (<∼0.1 V).[2,11,12] For the 2-DEG in III−V semiconductors, when the scale increases, the rectification decreases (as expected) due to a further shifting of the channel toward the diffusive regime.[8,9] However, rectification has

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Received for review December 17, 2014 and accepted May 11, 2015.

Published online May 11, 2015
10.1021/nn507199n

been observed when the V_0 increases even for micrometer-scale junctions.[8] At high V_0, for example, $V_0 >$ 1 V, the process can be understood so that the carriers associated with phonons are thermally emitted, losing their velocity during traveling, and they, consequently, can be accumulated near the anode (a positive-biased contact in the electron region and *vice versa* in the hole region). The accumulation yields a high resistivity, resulting in a stronger voltage drop in the channel,[8,14] enabling rectification even in the long-channel diffusive regime. This indicates that the sign of the potential shift is strongly dependent on the type of charge carriers. In a TTJ, consequently, positive output is generally expected in the hole region (as a positive rectification) and negative in the electron region (as a negative rectification).[30] Conventional III−V semiconductor based T-branch junction (TBJ) devices show negative rectifications, as they have only electrons as charge carriers.[7−10,13] Exceptionally, rectification whose sign is determined by the dimension and geometry of the junction scale has also been reported:[14] unexpectedly the rectification is changed from negative to positive when the channel width of the TBJ is more than ∼250 nm (but no more than a few micrometers). The origin of geometry-dependent rectification has not been confirmed, but may be associated with nonidentical potentials at the contacts.[14,31] Nevertheless, the sign of rectification is predetermined by the physical device's parameters and is not controllable during device operation. Graphene-based devices, on the other hand, exhibit both positive and negative rectifications by the gate field control.[25−27] So far, nonlinear behaviors have been studied for rectification only in nanoscale graphene TBJs (channel width ∼50−300 nm), minimizing the scattering events in carrier transport toward the ballistic effect.[25−30] Although they are very intriguing from an academic point of view and are promising for nanoelectronics, ballistic operations are impractical for flexible and transparent application owing to the strict nanoscale size requirements. In lithographically patterned nanostructures such as nanoribbons, however, carrier mobility is rather degraded due to additional scattering events associated with the imperfect edges.[32,33] Temperature- and substrate-induced scattering also limit the device viability. Therefore, the mean free path for nanoscale TBJs was observed in 20−130 nm at ambient condition.[26,27,29] Mobility is further degraded in the short channels by the high bias-induced doping effect.[34,35] As a result, the graphene nano-TBJs showed ∼5−12% maximum efficiency (V_{OUT}/V_{IN}) at room temperature.[26−29] In addition, the nanoscale devices displayed rectification curves that are asymmetric, which lowers the average value of the waveform.

Large-scale graphene prepared by CVD has the potential to deliver true monolithic integrated circuits (ICs), as one continuous monolayer graphene film can be utilized as a channel, gate, and interconnect, and even as passive components such as resistors and planar waveguides.[36] An all-graphene architecture would also significantly reduce the number of graphene−metal interfaces.[37] In order to capitalize on the full potential of transparent and flexible graphene, thin-film device architectures are needed, for example, for seamless integration of electronics. Therefore, it is worth studying the behavior of devices fabricated utilizing CVD graphene for future nanoelectronics.

In this study, we demonstrate a prominent room-temperature rectification in three-terminal all-graphene micrometer-scale devices. Thin-film devices realized as both channels and gate electrodes are fabricated utilizing CVD graphene. Highly tunable and switchable full-wave rectification for 100 kHz of ac input arising in the microscale TBJ is presented. A significant difference from the previous graphene TBJs is that here the local gate is applied only for the channel, instead of a global backgate, which can affect the conductivity of the center branch as well as contact resistance. The TBJ structure is further compared to a device having an invasive metal center probe to study the nonlinear effects along the two-terminal graphene channel. The rectification characteristics are explained using a diffusive model to provide insight into the device operation, which is based on self-gating by input voltages. These thin-film all-graphene devices, on the other hand, can also be used as high-performance inverters by simply changing the electrical configuration. Finally, we introduce a cascading all-graphene structure operating without an external gate field. The devices in separate layers are vertically configured in a way that the output of the first TBJ is utilized as a gate input of the second TBJ. As a result, apparent symmetric rectification from the second TBJ is observed without applying any gate voltage. This is a significant step toward practical graphene-based rectifiers as well as other electronic devices (like ring-oscillators) overcoming the zero-band-gap limit of graphene.

RESULTS AND DISCUSSION

Field-effect transistors (FETs) were fabricated utilizing graphene synthesized by photothermal CVD.[38] To assess the three-terminal-based operation, the devices were first structured with a metal as the center probe crossing the whole channel, as shown in Figure 1a and b. CVD graphene was utilized also as a gate electrode to replace the conventional metal electrode. We expect that the resistivity of the gate is not significant here since only direct current (dc) is employed through the gate in the rectifier device characterization, but for high-frequency applications the gate resistivity needs to be considered to avoid time delay of the signal. Channel length and width are 28 and 54 μm, respectively. In this paper, channel length is used to refer to the whole graphene channel between left and right metal terminals. The width of the center metal probe, if utilized, is always 0.5 μm regardless of the channel

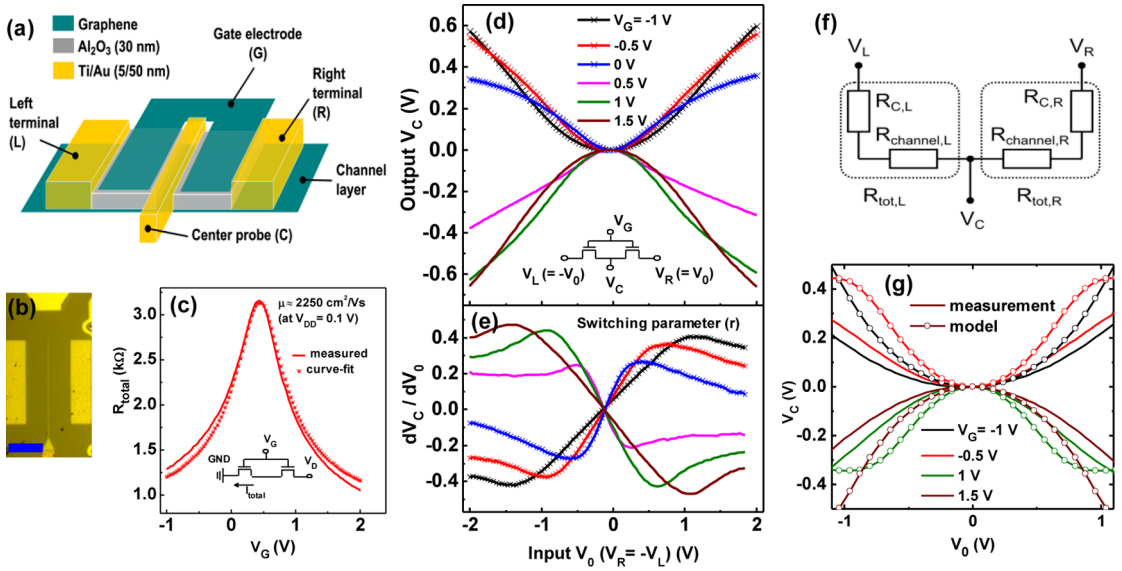

Figure 1. (a) Schematic and (b) optical image of a three-terminal graphene field-effect device. Scale bar is 20 μm. (c) Total resistance as a function of the gate voltage. Plots with the symbols are the values fitted to the measured values (solid line). (d−g) Rectifier operation: (d) output voltages detected at the center probe (V_C) for push−pull input (V_0) under different gate fields (V_G). V_0 is equivalent to V_R when the antisymmetric input V_L is applied to the other terminal. (e) Switching parameters r (=dV_C/dV_0) corresponding to the voltage transfer curves in (d). Lines with the symbols denote the outputs detected in the hole transport region. (f) Circuit diagram used to model the rectification characteristics. (g) Comparison of measured (solid line) and calculated (solid lines with symbols) rectification curves. Diagrams in the panels depict electrical configuration for each measurement.

dimensions. Raman mapping analysis was used to confirm that both layers are single-layer graphene (Figure S1 in the Supporting Information) and they are overlapped.[39,40] For device operation the left (L) and right (R) terminals were utilized for the input bias, and the center terminal (C) was used for the output signal detection (as described in Figure 1a). To identify the electrical properties of the graphene channel, the right terminal was biased (and the left was grounded) and the current flowing through the whole channel was monitored while the gate field was varied. As depicted in the inset of Figure 1c, the configuration is similar for inverter operation, as one terminal is connected to the power supply (V_{DD}) and the other is grounded (GND).[41,42] Figure 1c shows the measured total resistance (R_{total}) as a function of the gate voltage (V_G), indicating that the channel layer is slightly p-doped. Through curve-fitting to the measured data,[43] carrier mobility (μ) and carrier density at the charge neutral point (n_0) for the channel were extracted to be ~2250 cm^2/(V s) and ~6×10^{11} cm^{-2}, respectively.

For nonlinearity analysis, the electrical configuration of the channel was set up for push−pull applications, *i.e.*, complementary bias between the left and right terminals ($V_L = -V_R$). The schematic of the electrical configuration is shown in the inset of Figure 1d. During push−pull voltage (V_0) sweep, various gate voltages from −1 to 1.5 V were simultaneously applied. Figure 1d shows the output voltages detected at the center branch (V_C) with different gate voltages in the push−pull application. The output V_C clearly increases when the input $|V_0|$ ($V_R = V_0$ and $V_L = -V_0$) is increased and is unidirectional regardless of the sign of the input, exhibiting electrical rectification. Moreover, the output levels and signs are strongly dependent on the carrier type. In the region of -1 V < V_0 < 1 V the outputs are maximized at $V_G = -0.5$ V (hole transport region) for positive rectification and at V_G = 1 V (electron transport region) for negative rectification, respectively. In contrast, in the higher V_0 region (for example, V_0 > 1 V or V_0 < −1 V), at V_G = −0.5 and 1 *V* the output starts to saturate as the curvature becomes nonparabolic, which we attribute to the degradation of the conductivity of graphene in the high V_0 regime due to charge trapping in SiO_2.[34,35]

We evaluate the rectification with a switching parameter r (= dV_C/dV_0), as it relates to the efficiency, reveals the saturation points, and displays if the rectification has a parabolic nature. The results in Figure 1e show that the parameter r is increased linearly in the range of -1 V < V_0 < 1 V. The linear range corresponds perfectly to the parabolic rectification curve ($V_C \propto V_0^2 \rightarrow r \propto 2V_0$). Maximum $|r|$, about 0.45, is observed at around $V_0 = \pm 1$ V. By further increasing the gate electric field, on the other hand, the point of $|r|_{Max}$ is shifted toward the higher V_0 region without significant change in the magnitude. This indicates that the V_C is maximized with lowest carrier density near the conductance minima, *i.e.*, the Dirac point (V_{Dirac}), although it becomes almost zero at the Dirac point. The results are intriguing when considering that rectification is achieved while using an invasive metal center probe to

detect the center potential (V_C). In traditional nanoscale T-branch devices the rectification is explained typically through the ballistic junction effect associated with the center branch, which is not valid here, as there is no such T-branch junction. Furthermore, a device having dimensions of tens of micrometers on SiO_2/Si operates in the diffusive regime at room temperature.

To understand the rectifying characteristics in the large-scale graphene channel, we consider here device operation under diffusive transport with a two-terminal channel. Therefore, the classical field-effect-induced capacitive model can be applied because the device shown here utilizes the local gate (only for the channel area). This is another significant difference from previous graphene TBJs where global backgating was applied.[25−27,31] The global backgate modulates the conductivity of the graphene center probe as well as graphene−metal junctions,[37] which play a role in determining the rectification characteristics. Such field-effect-induced modulation can even reverse the sign of rectification.[31] In the case of thin-gate dielectrics the effective electric field is affected by the source−drain voltage.[44,45] The gate is floating during push−pull application, and consequently, the channel is associated with the self-gating from the biases with a magnitude of $\pm V_0$. Therefore, for the push−pull bias input (V_0) the effective gate voltages for the left and right channels can be expressed as $V_{eff,L} = V_G - V_{Dirac} + V_0$ and $V_{eff,R} = V_G - V_{Dirac} - V_0$, respectively, where V_{Dirac} is the gate voltage at the Dirac point. Considering the parallel plate capacitor model, which is commonly applied for graphene field-effect devices, $C = \varepsilon_0\varepsilon_r A/d = \alpha Ae$ and $n_{ind} = \alpha(V_G - V_D)$, where $\alpha = \varepsilon_0\varepsilon_r/de$, C is capacitance, ε_0 and ε_r are the permittivity of free space and dielectric medium, respectively, d is the thickness of the dielectric layer, A is the area, and e is the electron charge. The induced carrier concentration is defined as $n_{ind,i} = \alpha V_{eff,i}$ (i = L or R). This shows that the carrier concentration is symmetric in the left and right channels only at the Dirac point, whereas the applied gate bias ($V_G - V_D \neq 0$) results in asymmetric carrier concentration and, consequently, asymmetric conductivity between the left and right channels. For simplicity, we assume in our model that (i) the conductivity minimum (σ_{min}) and mobility (μ) are not affected by the drain−source bias, (ii) the carrier transport between the left and right channels is symmetric, and (iii) the metal contacts are identical. Instead of assuming negligible contact resistance, we include it in the total resistance, $R_{tot} = 2R_C + R_{channel}$, where the channel resistance is calculated using the gate voltage induced carrier concentration as $R_{channel} = L/(W\mu e(n_0^2 + n_{ind}^2)^{1/2})$, where L is the length, W the width, and n_0 the intrinsic carrier concentration.[43] As depicted in the circuit diagram for the model in Figure 1f, the output voltage can be expressed as $V_C = V_0(R_{tot,L} - R_{tot,R})/(R_{tot,L} + R_{tot,R})$. The calculated rectification characteristics are very similar to experimental results, as can be observed in Figure 1g. We assume that the small deviation arises from the shift of the Dirac point due to increased input bias V_0. The effect of the supply voltage V_{DD} on the channel conductivity is shown in Figures S3 and S13. In a graphene channel in which the intrinsic carrier concentration is negligible ($n_0 \ll n_{ind}$) the channel resistance is primarily determined by the field effect ($R_{channel} \propto n_{ind} \propto V_{eff}$). In such case, the output voltage has a parabolic dependence on the input voltage ($V_C \propto V_0^2$), and consequently, the switching parameter shows linear dependence as noted ($r \propto V_0$) in Figure 1. In a device where the intrinsic carrier concentration is significant, the graphene channel has a diminished field effect, resulting in hindered rectification performance. For significantly high n_0 ($n_0 \gg n_{ind}$), the output voltage would show linear dependence on the input voltage ($V_C \propto V_0$).

To further demonstrate the viability of these field-effect devices, we also utilized them as logic inverters by connecting one terminal to the power source (V_{DD}) and the other to the ground. In these measurements V_G is the input and V_C is the output. The voltage gain $|A|$ ($=|dV_C/dV_G|$) for the inverter is 1.63 at $V_{DD} = 4$ V, as seen in Figure 2a. The gain $|A|$ is proportional to the supply voltage but starts to saturate when V_{DD} reaches around 4 V (see Figure S3). Figure 2b shows the digital waveforms operating at 100 kHz, measured at the highest gain point for $V_{DD} = 4$ V, which presents the operation as a logic inverter (note also Figure S3 for 100 Hz and 1 MHz). The input and output signals are not perfectly matched due to the intrinsic shift of the Dirac point ($V_{Dirac} \approx 0.4$ V). To observe the effect of channel scaling with respect to the rectifier and inverter performance, narrower channel structures were fabricated. Although the extracted field-effect mobility was as high as 4700 $cm^2/(V\ s)$ at the low-bias regime for the 4 μm channel device, in comparison to the 28 μm long device (in Figure 1), the operational performance of the shorter channel device as a rectifier and inverter is limited (the performances of a device with a 14 and 4 μm channel can be seen in Figures S4 and S5, respectively). For a 4 μm channel device, the $|r|_{Max}$ was lowered to about 0.12 (from 0.45) at $V_0 = 1$ V and $|A|_{Max}$ to 0.54 (from 1.45) at $V_{DD} = 3$ V, respectively. It results from p−n junctions forming in the vicinity of the metal contacts due to stronger charge traps in the oxide or graphene−oxide interface when increasing the source−drain voltage.[34,35] Figure 2c plots channel-length-dependent device characteristics, which were extracted from sets of devices. Here, the critical channel length for device performance can be observed at around 5 μm.

To investigate the viability of the demonstrated graphene field-effect devices for all-graphene circuits, we introduce an alternative device structure that replaces the invasive metal center probe with a patterned center line as depicted in Figure 3. The dimensions of the channel are the same as in the device in

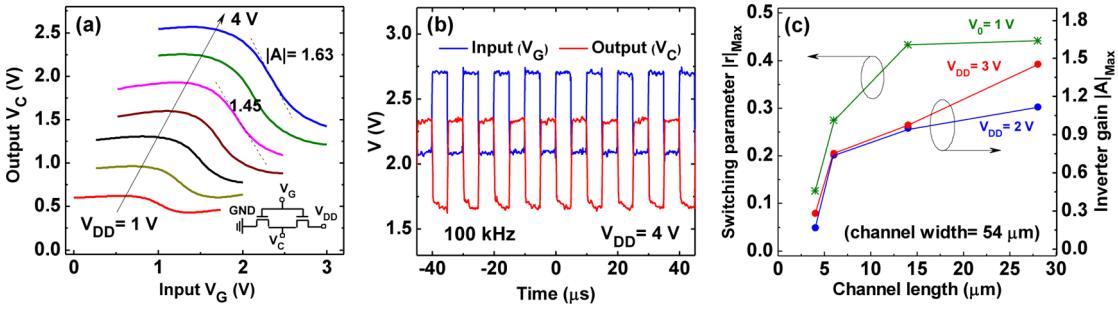

Figure 2. (a and b) Inverter operation of the three-terminal graphene field-effect device (shown in Figure 1): (a) dc transfer characteristics measured at the center terminal for the gate input with different supply voltages (from 1 to 4 V). (b) Digital output waveforms for the 100 kHz input signals at V_{DD} = 4 V. Diagram in the panel (a) depicts the electrical configuration for the measurement. (c) Channel scaling effect: performance of the three-terminal field-effect device *versus* channel length (4, 6, 14, and 28 μm). Maximum switching parameter for the rectifier in the region of -1 V < V_0 < 1 V and maximum voltage gain for inverters at V_{DD} = 3 V. The channel length denoted here is the distance between the left and right terminals. Channel width is 54 μm.

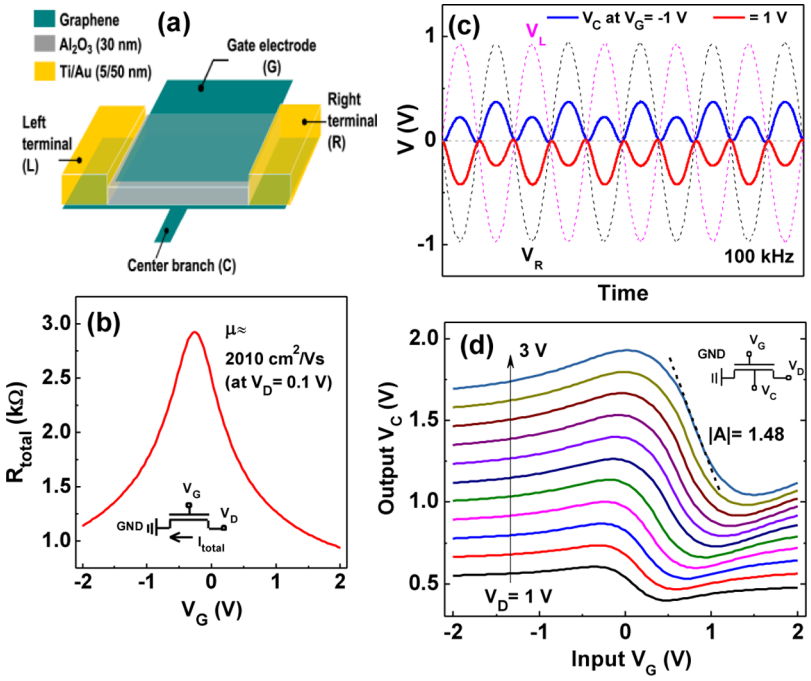

Figure 3. Characteristics of the TBJ (W/L = 54/28 μm) device. (a) Schematic of the TBJ. (b) Total resistance as a function of the gate voltage. (c) Rectifier operation: ac characteristics of the TBJ device for the 100 kHz push−pull inputs (dotted lines) under two different dc gate fields. The sinusoids (solid lines) in blue and red are the outputs (V_C) in the hole (V_G = −1 V) and electron region (V_G = 1 V), respectively. (d) Inverter operation: dc transfer characteristics with different supply voltages (from 1 to 3 V). The diagrams in the panels depict the electrical configuration for each of the measurements.

Figure 1 (28 μm in length between the left and right terminals and 54 μm in width). The graphene center branch is 2 μm wide and 3 μm long. A Raman map of the 2D-band (shown in Figure S6) clearly identifies that all of the functional areas in the TBJ device are composed of uniform single-layer graphene.

In the device analysis, the Dirac point can be observed at $V_G \approx -0.25$ V (slightly n-doped) and the extracted field-effect mobility (μ) is ~2010 cm^2/(V s), as can be seen in Figure 3b. In rectifier operation, the device has the same characteristics as the device with an invasive metal center branch: positive rectification in the hole and negative rectification in the electron transport region. The highly symmetric rectification curves are also observed near the Dirac point (but not in the carrier puddle region, which is here considered roughly at -0.5 V < V_G < 0 V), and the parameter r is saturated to about ±0.45 (details in Figure S6). The results are in a good agreement with a theoretical study explaining behavior in graphene TBJs.[30] Figure 3c further shows full-wave rectifications at the center branch without critical time delay for 100 kHz of ac input (ac characteristics for frequencies of 100 Hz, 10 kHz, and 1 MHz are shown in Figure S7). The sign of the rectification wave is simply switched by changing the carrier type through the electrostatic control as expected.

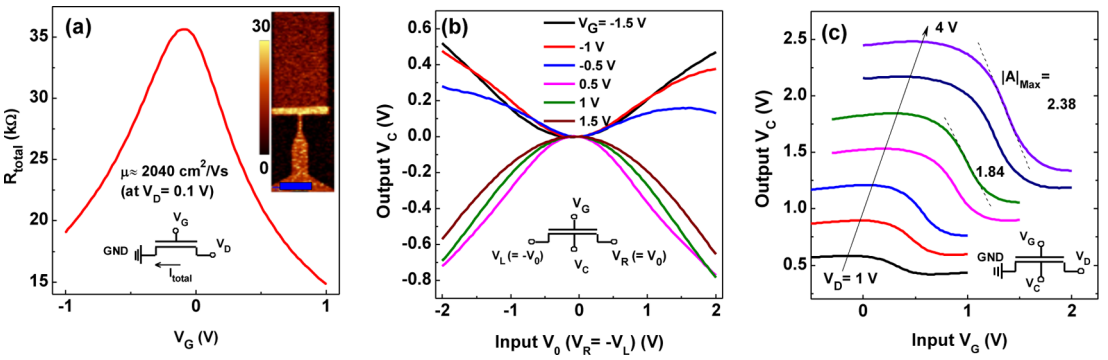

Figure 4. Characteristics of a device with a 4 μm channel width. (a) Total resistance as a function of the gate voltage (inset: Raman map of 2D-band for the area between L and R). The scale in the map is 20 μm. (b) Rectifier: output V_C for the push−pull voltage V_0 with different gate voltages. (c) Inverter: output V_C for the gate voltage V_G. All diagrams in the panels depict the electrical configuration for each of the measurements.

TABLE 1. Comparison of the Rectification Characteristics of Graphene TTJ/TBJ Devices Reported in Previous Studies[a]

					rectification			
ref	graphene material	scale W/L (μm)	V_0 (V)	V_G (V)	sign	$\|r\|_{Max}$	V_C/V_0 (max)	temp
25	exfoliated	∼0.2/0.2	0.1	±7	(+), (−)		∼2%	77 K
26	exfoliated	0.2/1.0	0.1	−6 to 7	(+), (−)	∼0.2	∼15%	RT
27	Exfoliated	0.3/0.45	0.05	−3 to 2	(+), (−)	∼0.14	∼13%	RT
28	epitaxial	0.03/0.5	2	N/A	(−)	0.4	23%	RT
29	epitaxial	0.02/0.4	1.5	N/A	(−)	0.4	23%	RT
here	CVD	4/28	2	−1.5 to 1.5	(+), (−)	0.5	38%	RT

[a] N/A: not applicable, (+) and (−) denote the positive and negative rectification, respectively.

The sinusoids in blue and red in Figure 3c denote the outputs (V_C) in the region of -1 V < V_0 < 1 V at V_G = -1 V (hole) and 1 V (electron), respectively. Operating the same device as an inverter, the maximum voltage gain ($|A|_{Max}$) at V_D = 3 V was about 1.5, as shown in Figure 3d. It is also similar to the device with an invasive metal center probe in Figure 1. Considering the device performances as a rectifier and inverter, the results point out that the graphene center branch performs adequately as a signal probe like a metal despite its much larger resistance compared to metal. This emphasizes that the graphene T-branch channel is a viable device concept enabling novel circuit architectures. Most of all, it allows the minimization of interfaces in circuitry while pursuing an all-graphene IC.

It is intriguing that nonlinear behavior presented as electrical rectification is observed in the CVD graphene channel on the scale of tens of micrometers in ambient air at room temperature. So far rectification has been considered to be enhanced in nanometer-scale TBJs due to possible high mobility and the fringing field effect.[30] To study the scaling of the channel width, we prepared a set of devices with varying widths from 4 to 54 μm. Figure 4 shows the characteristics of the device having a width of 4 μm (the devices with 28 and 14 μm channels can be seen in Figures S8 and S9, respectively).

The Dirac point is observed at about V_G = 0 V, and the extracted mobility is ∼2040 cm^2/(V s). For push−pull application the device performance is slightly enhanced: $|r|_{Max}$ is ∼0.5 at V_G = 1 V in the region of -1 V < V_0 < 1 V. The results are remarkable compared to previous reports on nanoscale devices,[25−29] when considering that here the much larger channel device is fabricated using photothermal CVD graphene having a small grain size (only a few micrometers).[38] Table 1 compares the rectifying performance of previously reported graphene TTJ/TBJ devices. For the inverter operation $|A|_{Max}$ of 1.84 and 2.38 is noted at V_D = 3 and 4 V, respectively (note characteristics of the second device in Figure S10, which shows $|A|_{Max}$ = 2.75 at V_D= 4 V, and comparison with other inverter devices in Table S1).

Although the best overall performance, *i.e.*, the highest values of $|r|$ and $|A|$, was observed at W/L = 4/28 μm, no significant trend affecting the device performance is found (the effect of the channel width scaling on the TBJ performance is shown in Figure S11). This observation is further confirmed by rather similar $R_{tot}W$ *versus* V_G curves for graphene devices with different channel widths (Figure S12). Because both the channel resistance ($R_{channel}$) and the contact resistance (R_C) scale with the width, the width cancels out in the fraction related to the voltage division when calculating the output voltage V_C and the switching parameter $|r|$ (in the rectification model above). Furthermore, in this work the mobilities were mostly found in the range 2000−3000 cm^2/(V s) with no observed correlation with the channel width. Therefore, in the diffusive transport regime, the performance of the device is

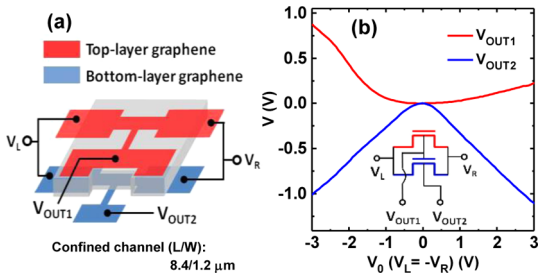

Figure 5. (a) Illustration of the thin-film circuit in which all-graphene devices are in two separate layers. The output graphene electrode of the first TBJ on the top layer is vertically aligned on the top of the channel of the TBJ on the bottom layer. (b) Output voltages of top-TBJ (V_{OUT1}) and bottom-TBJ (V_{OUT2}) for the common push−pull input voltage V_0. The inset shows the electrical configuration.

maximized when the channel is long enough (L > ~15 μm) to avoid performance degradation due to the high channel bias.

On the basis of the promising characteristics of the all-graphene devices, we fabricated a novel cascading structure utilizing two TBJs as illustrated in Figure 5 (details in Figure S14). Two TBJs are separated by 30 nm thick ALD Al_2O_3. The graphene output electrode of the first TBJ (on the top layer) is vertically aligned to function as the gate for the channel of the second TBJ (on the bottom). Both devices are patterned from a continuous CVD graphene film so that the center branch extends to the gate electrode. When measuring the device, the common push−pull input (V_0) was simultaneously applied to the cascading device structure as depicted in Figure 5a. Figure 5b shows the independently monitored output from the first TBJ (V_{OUT1}) and the second TBJ (V_{OUT2}). Relatively weak and asymmetric positive rectification was detected from the first TBJ device, indicating that the channel of the device is p-type. In contrast, very distinct and highly symmetric negative rectification (nearly V shaped) was observed from the second TBJ device. For V_{OUT2}, the switching parameter r saturates to about 0.4 at V_0 > 0.5 V and the efficiency reaches ~18% (V_C/V_0 ≈ 36%). It is obvious that the second TBJ is stimulated through the gate voltage generated by the first TBJ and, consequently, shows clear and stable rectification performance. The cascading device structure presents the possibility to design novel graphene devices based on a self-gating effect, *i.e.*, without employing the external gate bias. This could be applied for example as a two-terminal full-wave rectifier as an alternative to conventional semiconductor diodes (such as Schottky diodes), which have very high efficiency in rectification but generate only half-wave rectification with a single device.[46] We expect that these findings will open rich new possibilities for all-graphene circuits as the art develops.

CONCLUSIONS

In summary, highly operational room-temperature devices performing as a rectifier as well as inverter were demonstrated in this study utilizing three-terminal thin-film field-effect devices. To achieve the all-graphene device structure, the channel and gate were both fabricated using monolayer CVD graphene. Our findings open new possibilities for practical applications, as it was shown that ballistic nanoscale devices are not required to achieve rectifier characteristics. Consequently, instead of the ballistic theory, an electric-field-associated capacitive model was introduced to explain the rectification characteristics based on a self-gating effect. Highly tunable and switchable full-wave rectifications for a 100 kHz ac input was demonstrated in graphene T-branch junction devices. The same structure, on the other hand, can be utilized as a logic inverter by changing the electrical configuration. The highest output performance was observed at the longest and narrowest channel (W/L = 4/28 μm), which displayed switching parameter $|r|_{Max} \approx$ 0.5 and inverter voltage gain $|A|_{Max} \approx$ 2.8 at V_D = 4 V. Considering previous nanoscale three-terminal junction devices, the results obtained from the microscale thin-film devices are remarkable because they exhibit higher output efficiency (V_{OUT}/V_{IN}) despite operating in the diffusive transport regime. We finally introduced a cascading device structure using two identical microscale TBJs, where the output of the first TBJ is utilized as a gate input for the second TBJ. The measured output of the cascading structure showed very prominent rectification without any external gate. This is a significant step to realize the possibility of layer-by-layer device architecture for graphene-based monolithic ICs. It can be further expected that this paves the way for all-graphene thin-film applications and seamless flexible electronics.

METHODS

Graphene layers were grown on copper foil (~99.8%, Alfa Aesar) using photothermal chemical vapor deposition.[38] To synthesize single-layer graphene, the process was carried out at 935 °C in 60 s under ~11 mbar while introducing methane (12 sccm) and hydrogen (3 sccm) to the reactor. Prior to transfer, the film grown on the back side of the copper foil was removed by oxygen plasma. The graphene on the copper foil was coated with PMMA and floated on the solution of ammonium persulfate to etch the copper. The graphene film with PMMA was finally rinsed in deionized water and moved onto a 300 nm thick SiO_2/Si substrate. E-beam lithography was used for patterning in all device fabrication steps. During fabrication, the graphene channel was determined by first etching by oxygen plasma followed by 5/50 nm of Ti/Au metalization for contacts. Channel length was defined by the metal contacts of the left and right terminals. Afterward, 30 nm of Al_2O_3 was deposited by atomic layer deposition (ALD) on aluminum-seeded graphene. The second layer of graphene was transferred on the Al_2O_3-coated surface and patterned to define the top-gate electrode by O_2 plasma etching. To finalize the device structure, Ti/Au (5/50 nm) contact leads for the gate terminal were formed. In the device analysis, all measurements were carried out at room temperature in ambient air. An HP 4155A semiconductor parameter

analyzer was utilized for dc characteristics, and ac (high-frequency) characteristics were determined using an Agilent 33220A (as a signal generator) and HP 54845A (as an oscilloscope).

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Figures S1−S3: additional device characteristics for the 28 μm channel FET shown in Figure 1. Figures S4−S11: device performance with different dimensions (in width and length). Table S1: comparison of the graphene FETs operating as an inverter. Figure S12: resistivity with different channel widths ($R_{tot}W$). Figure S13: total resistances *versus* the gate voltage with varying V_{DD}. Figure S14: optical microscope and Raman images of the cascading TBJ device. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/nn507199n.

Acknowledgment. The research leading to these results has received funding from the European Union Seventh Framework Programme under grant agreement no. 604391 Graphene Flagship. This was undertaken at the Micronova, Nanofabrication Center of Aalto University. The authors also acknowledge the funding by the Academy of Finland, TEKES−the Finnish Funding Agency for Technology and Innovation.

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